REMARKS / ARGUMENTS

Claims 1-17 remain in the application, all of which stand rejected.

1. Rejection of Claims 1-5 and 7-16 Under 35 USC 102(b)

Claims 1-5 and 7-16 stand rejected under 35 USC 102(b) as being anticipated by Agrawal (US 5,257,268).

With respect to claim 1, the Examiner asserts that Agrawal discloses "determining a required memory needed to execute [a] plurality of test vectors" in col. 4:40-60, where Agrawal discloses a system that determines the minimum required number of flip-flops gates (memory). *See*, 3/15/2010 Final Office Action, p. 4. Applicants respectfully disagree.

Agrawal discloses that:

> . . .A sequential circuit. . .is fully initialized when all its memory elements are in known states. One has to provide a set of initialization vectors to bring a circuit to a known state, and those initialization vectors must be chosen appropriately. In accordance with our preferred embodiment, the initialization vectors are generated by a procedure that minimizes a "cost function". We chose our cost function to correspond to the number of flip-flops in the "unknown" state, but other cost functions are also possible.
>
> As shown in the flow chart of FIG. 2, the initialization process begins at block 100 with the assumption that all flip-flops are at the "unknown" state, and the cost function is simply equal to the number of flip-flops in the circuit, M. The process of selecting a set of initialization vectors consists of generating "trial vectors" and accepting only those trial vectors that reduce the cost.

Col. 4, lines 43-60.

From the above excerpt, applicants believe it is clear that Agrawal does not disclose an action of "determining a required memory needed to execute [a] plurality of test vectors". Instead, Agrawal discloses an action of determining a number of memory elements (flip-flops) that are affected (or initialized) by one or

more initialization vectors. The number of memory elements that are affected by (or *initialized by*) the application of one or more initialization vectors has no particular relationship to the number of memory elements that are *required to execute* a plurality of test vectors. For example, Agrawal indicates that any number of initialization vectors can be applied to a sequential circuit, but the application of additional initialization vectors may or may not cause more of the circuit's flip-flops to be initialized. Thus, Agrawal does not need to determine a required memory *needed* to execute a plurality of initialization vectors, but instead needs to determine how many flip-flops are *affected* when a set of initialization vectors is applied to a circuit. These two determinations are different.

In response to the above argument, the Examiner asserted that the phrase "required memory" is equal to the phrase "minimum number of flip-flops". *See*, 3/15/2010 Final Office Action, p. 3. Applicants respectfully disagree and assert that the Examiner is reading the phrase "required memory" out of context. To anticipate claim 1, Agrawal needs to disclose more than just the existence of a "required memory", and instead needs to disclose "determining a required memory needed to execute the plurality of test vectors". Agrawal does not disclose this.

Applicants note that the "number of flip-flops" referred to by Agrawal in col. 4:40-60 is a number of flip-flops in an unknown state, which number of flip-flops need to be initialized and tested. The number of flip-flops disclosed by Agrawal is not a number of flip-flops that is "required. . .to execute [a] plurality of test vectors", but is simply a number of flip-flops that exists to be tested. In the context of Agrawal, it makes no sense to read a test file having a plurality of test vectors and then determine "a required memory needed to execute the plurality of test vectors", because the number of flip-flops being tested is fixed irrespective of the test vectors. If anything, Agrawal needs to determine a required number of vectors for initializing or testing a known number of flip-flops.

Given that Agrawal does not disclose "determining a required memory needed to execute the plurality of test vectors", it follows that Agrawal cannot

disclose "using the required memory to estimate a cost to execute the test vectors." In particular, the "cost function" disclosed by Agrawal is not an estimated "cost to execute. . .[a plurality of] test vectors". Instead, Agrawal's "cost function" is an optimization tool that is used to limit growth in a set of initialization vectors. For example, in a simple case, an initialization vector is not added unless it actually causes additional flip-flops to be initialized optimum number of initialization vectors. Put another way, Agrawal's "cost function" is an optimization tool, not an estimation tool.

Because Agrawal does not disclose each and every recitation of applicants' claim 1, claim 1 is believed to be allowable.

Claims 2-5 and 7 are believed to be allowable, at least, because they depend from claim 1.

Claims 8-16 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

2. Rejection of Claims 6 and 17 Under 35 USC 103(a)

Claims 6 and 17 stand rejected under 35 USC 103(a) as being unpatentable over Agrawal.

Applicants' claims 6 and 17 are believed to be allowable, at least, because they respectively depend from claims 1 and 13.

3. Conclusion

Given the above Amendments and Remarks, applicants respectfully request the issuance of a Notice of Allowance.

Respectfully submitted,
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